REMARKS

Applicant is in receipt of the Office Action mailed November 1, 2005. New claim 44 has been added. Claims 1-44 are pending in the application.

35 U.S.C. § 102 Rejection:

Claims 1, 2, 4, 10-12, 16-18, 24-35, and 38-43 were rejected under 35 U.S.C. § 102(e) as being anticipated by Piau (U.S. Patent Publication No. 2004/0049627); (evidentiary reference: Blood et al (U.S. Patent Publication No. 2003/0110351)). Applicant respectfully traverses this rejection.

Independent claim 1 recites:

> A flash-memory card-reader system comprising:
> a hard disk controller interface;
> a buffer coupled to the hard disk controller interface;
> a processing unit coupled to the buffer; and
> a flash-memory card-controller unit coupled to the buffer and to the processing unit;
> wherein the hard disk controller interface is operable to communicate with a hard disk controller in a host system, wherein the hard disk controller interface is operable to receive incoming commands from the hard disk controller; and
> wherein the processing unit is operable to translate the incoming commands to produce translated incoming commands usable by the flash-memory card-controller unit, wherein the processing unit is operable to provide the translated incoming commands to the flash-memory card-controller unit.

Examiner states that Piau describes a flash-memory card-reader system – as illustrated in Fig. 2 – comprising all the elements recited in claim 1 of Applicant. Accordingly, Examiner states that #220 in Fig. 2 corresponds to the flash-memory card-controller unit recited in claim 1. Applicant submits that this characterization is in error, as it is clearly stated by Piau that #200 is itself the flash controller disclosed by Piau

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(paragraph 17, line 3). This is an important distinction relating to the functionality of the blocks described by Piau, and the overall functionality of the system proposed by Piau as opposed to the combination of features recited in claim 1. Because #200 operates as the flash controller, #220 is not capable of using commands usable by a flash-memory card-controller or a flash memory card, as the use of such commands is the function of #200. Commands usable by a flash-memory controller are well known to those skilled in the art, and may include commands such as 'erase block', 'read sequential', etc. These commands are not commensurate with simple read/write commands, as referred to by Examiner in referencing paragraphs 29 and 30 of Piau. Furthermore, Piau clearly states that Fig. 2 is a block diagram illustrating the operative components of a Compact Flash controller, not a system in which a flash-memory controller is coupled to other devices and/or components. In addition, the flash controller is specified as a Compact Flash controller, which is one specific type of flash-memory controller. Dependent claims 8, 9, 22, 23, 36 and 37 of Applicant are also indicative of such a distinction.

It is clear from Applicant's own Fig. 2 that the flash-memory card-controller(s) is (are) a component(s) in Applicant's system, and are not themselves considered to be the disclosed system. It is further clear that the equivalent of #200 from Fig. 2 of Piau is element #150 in Fig. 2 of Applicant. Since Piau specifically discloses a flash memory controller that is incorporated in a flash memory (see also Abstract of Piau), it is evident that #220 in Fig. 2 of Piau does not correspond to the flash-memory card-controller recited in claim 1, and the functionality of the system disclosed by Piau therefore differs from the combination of features recited in claim 1. Furthermore, as Piau presents a Compact Flash controller configured specifically for splitting data into odd segments and even segments (paragraph 18, lines 13-17), and transferring the data to two separate flash memory modules (paragraph 19, lines 15-19), there is no motivation or suggestion by Piau for configuring a flash-memory card-reader system in which a flash-memory card, which may be any one of a specified number of different flash-memory card types, appears as a hard disk drive to a host system.

For at least these reasons, Applicant submits that Piau does not disclose and/or suggest the combination of features recited in claim 1. Independent claims 16, 28, 31, and 38 were rejected based on the same rationale as in the rejection of claim 1.

Accordingly, for at least the same reasons as given above, Applicant further submits that Piau does not disclose and/or suggest the combination of features recited in claims 16, 28, 31, and 38. Applicant also submits that since the independent claims have been shown to be patentably distinct, dependent claims 2, 4, 10-12, 17-18, 24-30, 32-35, and 39-43 are also patentably distinct for at least the same reasons the independent claims are patentably distinct, and a further discussion of these dependent claims is not necessary at this time.

35 U.S.C. § 103 Rejection:

Claims 3, and 13-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Piau (U.S. Patent Publication No. 2004/0049627) as applied to claim 1, and further in view of Day et al (U.S. Patent Publication No. 2004/0049627). Claims 5-9, 19-23, and 36-37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Piau (U.S. Patent Publication No. 2004/0049627), Day et al (U.S. Patent Publication No. 2004/0049627) and further in view of Tsao (U.S. Patent Publication No. 2005/0029348). Applicant submits that because the independent claims on which the rejected dependent claims depend have been shown to be patentably distinct, these dependent claims are also patentably distinct for at least the same reasons the independent claims are patentably distinct, and a further discussion of these dependent claims is not necessary at this time.
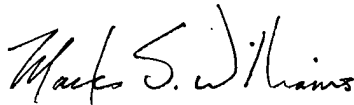
CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-15055707-05300/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,

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